Results for "((boolean satisfiability<and>cyclic)) <and> (pyr >= 1951 <and> pyr <= 2001)" e-mail
Your search matched **11** of **1250969** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» Search Options

View Session History

New Search

Modify Search

((boolean satisfiability<and>cyclic)) <and> (pyr >= 1951 <and> pyr <= 2001)

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information

1. **Exact algorithms for output encoding, state assignment, and four-level B minimization**
Devadas, S.; Newton, A.R.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 10, Issue 1, Jan. 1991 Page(s):13 - 27
Digital Object Identifier 10.1109/43.62788
AbstractPlus | Full Text: PDF(1476 KB) IEEE JNL

2. **Local search for satisfiability (SAT) problem**
Gu, J.;
Systems, Man and Cybernetics, IEEE Transactions on
Volume 23, Issue 4, July-Aug. 1993 Page(s):1108 - 1129
Digital Object Identifier 10.1109/21.247892
AbstractPlus | Full Text: PDF(1752 KB) IEEE JNL

3. **Test generation for cyclic combinational circuits**
Raghunathan, A.; Ashar, P.; Malik, S.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 14, Issue 11, Nov. 1995 Page(s):1408 - 1414
Digital Object Identifier 10.1109/43.469666
AbstractPlus | Full Text: PDF(636 KB) IEEE JNL

4. **Hazard-free implementation of speed-independent circuits**
Kondratyev, A.; Kishinevsky, M.; Yakovlev, A.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 17, Issue 9, Sept. 1998 Page(s):749 - 771
Digital Object Identifier 10.1109/43.720313
AbstractPlus | References | Full Text: PDF(600 KB) IEEE JNL

5. **IGRAINE-an Implication GRaph-bAsed engINE for fast implication, justific propagation**
Tafertshofer, P.; Ganz, A.; Antreich, K.J.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 19, Issue 8, Aug. 2000 Page(s):907 - 927
Digital Object Identifier 10.1109/43.856977
AbstractPlus | References | Full Text: PDF(660 KB) IEEE JNL

6. **An efficient heuristic approach to solve the unate covering problem**
Cordone, R.; Ferrandi, F.; Sciuto, D.; Calvo, R.W.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 20, Issue 12, Dec. 2001 Page(s):1377 - 1388
Digital Object Identifier 10.1109/43.969431

AbstractPlus | References | Full Text: PDF(263 KB) IEEE JNL

7. **Symbolic simulation techniques-state-of-the-art and applications**
Blank, C.; Eveking, H.; Levihn, J.; Ritter, G.;
High-Level Design Validation and Test Workshop, 2001. Proceedings. Sixth IE
7-9 Nov. 2001 Page(s):45 - 50
Digital Object Identifier 10.1109/HLDVT.2001.972806
AbstractPlus | Full Text: PDF(117 KB) IEEE CNF

8. **A decision procedure for bit-vector arithmetic**
Barrett, C.W.; Dill, D.L.; Levitt, J.R.;
Design Automation Conference, 1998. Proceedings
15-19 Jun 1998 Page(s):522 - 527
AbstractPlus | Full Text: PDF(604 KB) IEEE CNF

9. **Using reconfigurable computing techniques to accelerate problems in th case study with Boolean satisfiability**
Peixin Zhong; Ashar, P.; Malik, S.; Martonosi, M.;
Design Automation Conference, 1998. Proceedings
15-19 Jun 1998 Page(s):194 - 199
AbstractPlus | Full Text: PDF(588 KB) IEEE CNF

10. **Robust encodings in genetic algorithms: a survey of encoding issues**
Ronald, S.;
Evolutionary Computation, 1997., IEEE International Conference on
13-16 April 1997 Page(s):43 - 48
Digital Object Identifier 10.1109/ICEC.1997.592265
AbstractPlus | Full Text: PDF(668 KB) IEEE CNF

11. **Some recent advances in software and hardware logic simulation**
Murgai, R.; Fujita, M.;
VLSI Design, 1997. Proceedings., Tenth International Conference on
4-7 Jan. 1997 Page(s):232 - 238
Digital Object Identifier 10.1109/ICVD.1997.568081
AbstractPlus | Full Text: PDF(648 KB) IEEE CNF

Results for "(path sensitization) <and> (pyr >= 1951 <and> pyr <= 2001)"
Your search matched **201** of **1250969** documents.
A maximum of **250** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

e-mail

» Search Options

View Session History

New Search

Modify Search

(path sensitization) <and> (pyr >= 1951 <and> pyr <= 2001)

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information View: **1-25** | 26-50 | 51-75 | 76-100

1. **Path sensitization in critical path problem [logic circuit design]**
Chen, H.-C.; Du, D.H.-C.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 12, Issue 2, Feb. 1993 Page(s):196 - 207
Digital Object Identifier 10.1109/43.205001
AbstractPlus | Full Text: PDF(1064 KB) IEEE JNL

2. **DYNAMITE: an efficient automatic test pattern generation system for patl**
Fuchs, K.; Fink, F.; Schulz, M.H.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 10, Issue 10, Oct. 1991 Page(s):1323 - 1335
Digital Object Identifier 10.1109/43.88928
AbstractPlus | Full Text: PDF(1172 KB) IEEE JNL

3. **RESIST: a recursive test pattern generation algorithm for path delay fault various test classes**
Fuchs, K.; Pabst, M.; Rossel, T.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 13, Issue 12, Dec. 1994 Page(s):1550 - 1562
Digital Object Identifier 10.1109/43.331411
AbstractPlus | Full Text: PDF(1160 KB) IEEE JNL

4. **Efficient timing analysis for CMOS circuits considering data dependent d**
Shang-Zhi Sun; Du, D.H.C.; Hsi-Chuan Chen;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 17, Issue 6, June 1998 Page(s):546 - 552
Digital Object Identifier 10.1109/43.703835
AbstractPlus | References | Full Text: PDF(184 KB) IEEE JNL

5. **The calculation of signal stable ranges in combinational circuits**
Liu, L.-R.; Chen, H.-C.; Du, D.H.C.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 13, Issue 8, Aug. 1994 Page(s):1016 - 1023
Digital Object Identifier 10.1109/43.298037
AbstractPlus | Full Text: PDF(732 KB) IEEE JNL

6. **Performance optimization by gate sizing and path sensitization**
Kim, J.; Du, D.H.C.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 17, Issue 5, May 1998 Page(s):459 - 462
Digital Object Identifier 10.1109/43.703945

AbstractPlus | References | Full Text: PDF(128 KB) IEEE JNL

7. **Primitive path delay faults: identification and their use in timing analysis**
Sivaraman, M.; Strojwas, A.J.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 19, Issue 11, Nov. 2000 Page(s):1347 - 1362
Digital Object Identifier 10.1109/43.892858
AbstractPlus | References | Full Text: PDF(332 KB) IEEE JNL

8. **Efficient logic-level timing analysis using constraint-guided critical path :**
Chanhee Oh; Mercer, M.R.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 4, Issue 3, Sept. 1996 Page(s):346 - 355
Digital Object Identifier 10.1109/92.532035
AbstractPlus | References | Full Text: PDF(960 KB) IEEE JNL

9. **Hierarchical path sensitization for testability analysis and DFT**
Micallef, S.P.; Moore, W.R.;
Design for Testability, IEE Colloquium on
16 May 1991 Page(s):7/1 - 7/8
AbstractPlus | Full Text: PDF(552 KB) IEE CNF

10. **Path sensitisation and gate sizing approach to low power optimisation**
Juho Kim; Jaesok Yang; Sun-Young Hwang;
Electronics Letters
Volume 34, Issue 7, 2 April 1998 Page(s):619 - 620
AbstractPlus | Full Text: PDF(236 KB) IEE JNL

11. **Critical path selection for performance optimization**
Chen, H.-C.; Du, D.H.-C.; Liu, L.-R.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 12, Issue 2, Feb. 1993 Page(s):185 - 195
Digital Object Identifier 10.1109/43.205000
AbstractPlus | Full Text: PDF(980 KB) IEEE JNL

12. **An efficient parallel critical path algorithm**
Li-Ren Liu; Du, D.H.C.; Hsi-Chuan Chen;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 13, Issue 7, July 1994 Page(s):909 - 919
Digital Object Identifier 10.1109/43.293948
AbstractPlus | Full Text: PDF(1088 KB) IEEE JNL

13. **A fast nonenumerative automatic test pattern generator for path delay fa**
Tragoudas, S.; Karayiannis, D.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 18, Issue 7, July 1999 Page(s):1050 - 1057
Digital Object Identifier 10.1109/43.771185
AbstractPlus | References | Full Text: PDF(184 KB) IEEE JNL

14. **Sensitisable-path-oriented clustered voltage scaling technique for low pc**
Jou, J.-Y.; Chou, D.-S.;
Computers and Digital Techniques, IEE Proceedings-
Volume 145, Issue 4, July 1998 Page(s):301 - 307
AbstractPlus | Full Text: PDF(644 KB) IEE JNL

15. **An efficient algorithm for sequential circuit test generation**
Kelsey, T.P.; Saluja, K.K.; Lee, S.Y.;
Computers, IEEE Transactions on
Volume 42, Issue 11, Nov. 1993 Page(s):1361 - 1371
Digital Object Identifier 10.1109/12.247839
AbstractPlus | Full Text: PDF(1108 KB) IEEE JNL

16. **Path sensitization in critical path problem**
Chen, H.-C.; Du, D.H.C.;
Computer-Aided Design, 1991. ICCAD-91. Digest of Technical Papers., 1991 I Conference on
11-14 Nov. 1991 Page(s):208 - 211
Digital Object Identifier 10.1109/ICCAD.1991.185233
AbstractPlus | Full Text: PDF(336 KB) IEEE CNF

17. **The complexity of the inclusion operation on OFDD's**
Drechsler, R.; Sauerhoff, M.; Sieling, D.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 17, Issue 5, May 1998 Page(s):457 - 459
Digital Object Identifier 10.1109/43.703943
AbstractPlus | References | Full Text: PDF(80 KB) IEEE JNL

18. **Automatic synthesis of large telescopic units based on near-minimum tir**
Benini, L.; De Micheli, G.; Lioy, A.; Macii, E.; Odasso, G.; Poncino, M.;
Computers, IEEE Transactions on
Volume 48, Issue 8, Aug. 1999 Page(s):769 - 779
Digital Object Identifier 10.1109/12.795120
AbstractPlus | References | Full Text: PDF(360 KB) IEEE JNL

19. **Multiple path sensitization for hierarchical circuit testing**
Chau-Chin Su; Kime, C.R.;
Test Conference, 1990. Proceedings., International
10-14 Sept. 1990 Page(s):152 - 161
Digital Object Identifier 10.1109/TEST.1990.114013
AbstractPlus | Full Text: PDF(928 KB) IEEE CNF

20. **Fast true delay estimation during high level synthesis**
Bhattacharya, S.; Dey, S.; Brglez, F.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 15, Issue 9, Sept. 1996 Page(s):1088 - 1105
Digital Object Identifier 10.1109/43.536715
AbstractPlus | References | Full Text: PDF(1824 KB) IEEE JNL

21. **Realistic delay modeling in satisfiability-based timing analysis**
e Silva, L.G.; Marques Silva, J.P.; Silveira, L.M.; Sakallah, K.A.;
Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE Interna on
Volume 6, 31 May-3 June 1998 Page(s):215 - 218 vol.6
Digital Object Identifier 10.1109/ISCAS.1998.705250
AbstractPlus | Full Text: PDF(456 KB) IEEE CNF

22. **Fundamentals of testability-a tutorial**
Fritzemeier, R.R.; Nagle, H.T.; Hawkins, C.F.;
Industrial Electronics, IEEE Transactions on
Volume 36, Issue 2, May 1989 Page(s):117 - 128
Digital Object Identifier 10.1109/41.19061
AbstractPlus | Full Text: PDF(1268 KB) IEEE JNL

23. **SCRIPT: a critical path tracing algorithm for synchronous sequential circ**
Menon, P.; Levendel, Y.; Abramovici, M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 10, Issue 6, June 1991 Page(s):738 - 747
Digital Object Identifier 10.1109/43.137502
AbstractPlus | Full Text: PDF(980 KB) IEEE JNL

24. **On variable clock methods for path delay testing of sequential circuits**
Chakraborty, T.J.; Agrawal, V.D.; Bushnell, M.L.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction

Volume 16, Issue 11, Nov. 1997 Page(s):1237 - 1249
Digital Object Identifier 10.1109/43.663815

AbstractPlus | References | Full Text: PDF(228 KB) IEEE JNL

25. **Functional vector generation for HDL models using linear programming a satisfiability**
Fallah, F.; Devadas, S.; Keutzer, K.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 20, Issue 8, Aug. 2001 Page(s):994 - 1002
Digital Object Identifier 10.1109/43.936380

AbstractPlus | References | Full Text: PDF(152 KB) IEEE JNL

[redacted]

View: **1-25** | 26-50 | 51-75 | 76-100

Terms used **path sensitization** and **cyclic** Found **4,282** of **166,357**

Sort results by relevance Save results to a Binder Try an Advanced Search

Display results expanded form Search Tips Try this search in The ACM Guide

Open results in a new window

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Best 200 shown Relevance scale

1 Non-Enumerative Path Delay Fault Diagnosis

Saravanan Padmanaban, Spyros Tragoudas

March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**

Publisher: IEEE Computer Society

Full text available: pdf(211.24 KB) Publisher Site Additional Information: full citation, abstract, index terms

The first non-enumerative framework for diagnosing path delay faults using zero suppressed binary decision diagrams is introduced. We show that fault free path delay faults with a validated non-robust test may together with fault free robustly tested faults be used to eliminate faults from the set of suspected faults. All operations are implemented by an implicit diagnosis tool based on the zero suppressed binary decision diagram. The proposed method is space and time non-enumerative as opposed ...

2 Analysis of cyclic combinational circuits

Sharad Malik

November 1993 **Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society Press

Full text available: pdf(770.89 KB) Additional Information: full citation, references, citings

3 Session S3.1: architecture adaptation and synthesis: Cycle-time aware architecture synthesis of custom hardware accelerators

Mukund Sivaraman, Shail Aditya

October 2002 **Proceedings of the 2002 international conference on Compilers, architecture, and synthesis for embedded systems**

Publisher: ACM Press

Full text available: pdf(75.23 KB) Additional Information: full citation, abstract, references, index terms

We present the cycle-time aware architecture synthesis methodology used in PICO-NPA that automatically synthesizes minimal cost RT-level designs from high-level specifications to meet a given cycle-time. This allows subsequent physical synthesis to succeed on first pass with predictable performance. The core of the methodology is a static timing analysis engine that is used at multiple levels - program-level, architecture-level and RT-level - in order to identify, schedule and validate useful op ...

Keywords: clock frequency, delay analysis, embedded hardware architecture synthesis, high-level synthesis, operator chaining, target clock period, timing analysis, timing during scheduling

4 Oscillation control in logic simulation using dynamic dominance graphs

Peter Dahlgren
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(125.57 KB) Additional Information: full citation, references, index terms

5 Desensitization for power reduction in sequential circuits

Xiangfeng Chen, Peicheng Pen, C. L. Liu
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(183.09 KB) Additional Information: full citation, references, index terms

6 Tutorial: Compiling concurrent languages for sequential processors

Stephen A. Edwards
April 2003 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 8 Issue 2
Publisher: ACM Press
Full text available: pdf(771.65 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Embedded systems often include a traditional processor capable of executing sequential code, but both control and data-dominated tasks are often more naturally expressed using one of the many domain-specific concurrent specification languages. This article surveys a variety of techniques for translating these concurrent specifications into sequential code. The techniques address compiling a wide variety of languages, ranging from dataflow to Petri nets. Each uses a different method, to some degr ...

Keywords: Compilation, Esterel, Lustre, Petri nets, Verilog, code generation, communication, concurrency, dataflow, discrete-event, partial evaluation, sequential

7 Automated multi-cycle symbolic timing verification of microprocessor-based designs

Anurag P. Gupta, Daniel P. Siewiorek
June 1994 **Proceedings of the 31st annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(140.84 KB) Additional Information: full citation, references, citings, index terms

8 Functional vector generation for HDL models using linear programming and 3-satisfiability

Farzan Fallah, Srinivas Devadas, Kurt Keutzer
May 1998 **Proceedings of the 35th annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(252.59 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Our strategy for automatic generation of functional vectors is based on exercising selected paths in the given hardware description language (HDL) model. The HDL model describes interconnections of arithmetic, logic and memory modules. Given a path in the HDL model, the search for input stimuli that exercise the path can be converted into a standard satisfiability checking problem by expanding the arithmetic modules into logic-gates. However, this approach is not very efficient. ...

Keywords: MPEG4, codec, design automatian, flip-flops, level converters, low power, placement, synthesis, voltage scaling

9 Digital test generation and design for testability

John Grason, Andrew W. Nagle
June 1980 **Proceedings of the 17th conference on Design automation**
Publisher: ACM Press

Full text available: pdf(1.42 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper is a tutorial intended primarily for individuals just getting started in digital testing. Basic concepts of testing are described, and the steps in the test development process are discussed. A pragmatic approach to test sequence generation is presented, oriented towards ICs interconnected on a board. Finally, design for testability techniques are described, with an emphasis on solving problems that appeared during the test generation discussion.

10 SAT based ATPG using fast justification and propagation in the implication graph

Paul Tafertshofer, Andreas Ganz
November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Press

Full text available: pdf(179.42 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we present new methods for fast justification and propagation in the implication graph (IG) which is the core data structure of our SAT based implication engine. As the IG model represents all information on the implemented logic function as well as the topology of a circuit, the proposed techniques inherit all advantages of both general SAT based and structure based approaches to justification, propagation, and implication. These three fundamental Boolean problems are ...

11 Design methodologies for noise in digital integrated circuits

Kenneth L. Shepard
May 1998 **Proceedings of the 35th annual conference on Design automation**
Publisher: ACM Press

Full text available: pdf(222.60 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

In this paper, we describe the growing problems of noise in digital integrated circuits and the design tools and techniques used to ensure the noise immunity of digital designs.

Keywords: high-level synthesis, telecommunication

12 Functional testing techniques for digital LSI/VLSI systems

Stephen Y.H. Su, Tonysheng Lin
June 1984 **Proceedings of the 21st conference on Design automation**
Publisher: IEEE Press

Full text available: pdf(1.39 MB) Additional Information: full citation, abstract, references, citings, index terms

Functional testing is becomilng more important due to the increasing complexity in digital LSI/VLSI devices. Various functional testing approaches have been proposed to meet this urgent need in LSI/VLSI testing. This paper presents the basic ideas behind deterministic functional testing and concisely overviews eight major functional testing techniques. Comparisons among these techniques and suggestions for future development are made to meet the challenges in this fast growing testing field ...

13 Power management techniques for control-flow intensive designs

Anand Raghunathan, Sujit Dey, Niraj K. Jha, Kazutoshi Wakabayashi
June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**
Publisher: ACM Press
Full text available: pdf(187.17 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper presents a low-overhead controller-based powermanagement technique that re-specifies control signals to reconfigureexisting multiplexer networks and functional units to minimizeunnecessary activity. We demonstrate that conventional powermanagement techniques may often not be suited to control-flowintensive designs, and provide a comprehensive analysis of thepotential negative effects of power management on circuit delay,glitching activity at control and data path signals, and formatio ...

14 Analyzing cycle stealing on synchronous circuits with level-sensitive latches

I. Lin, J. A. Ludwig, K. Eng
July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**
Publisher: IEEE Computer Society Press
Full text available: pdf(685.55 KB) Additional Information: full citation, references, citings, index terms

15 Complexity of sequential ATPG

T. E. Marchok, A. El-Maleh, W. Maly, J. Rajski
March 1995 **Proceedings of the 1995 European conference on Design and Test**
Publisher: IEEE Computer Society
Full text available: pdf(1.20 MB) Publisher Site Additional Information: full citation, abstract, citings

The research reported in this paper was conducted to identify those attributes, of both sequential circuits and structural, sequential automatic test pattern generation (ATPG) algorithms, which can lead to extremely high test generation times. The retiming transformation is used as a mechanism to create two classes of circuits which present varying degrees of complexity for test generation. It was observed for three different sequential test generators that the increase in complexity of testing ...

Keywords: VLSI, automatic test pattern generation, automatic testing, circuit attribute, density of encoding, design for testability, integrated circuit testing, logic testing, retiming transformation, sequential ATPG, sequential circuits, structural ATPG, test generation times, testing complexity, timing

16 Path sensitization of combinational circuits and its impact on clocking of sequential systems

R. Peset Llopis
December 1995 **Proceedings of the conference on European design automation**
Publisher: IEEE Computer Society Press
Full text available: pdf(672.15 KB) Additional Information: full citation, references, index terms

17 VIPER: an efficient vigorously sensitizable path extractor

Hoon Chang, Jacob A. Abraham
July 1993 **Proceedings of the 30th international conference on Design automation**
Publisher: ACM Press
Full text available: pdf(766.04 KB) Additional Information: full citation, references, citings, index terms

18 Provably correct high-level timing analysis without path sensitization

Subhrajit Bhattacharya, Sujit Dey, Franc Brglez

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society Press

Full text available: pdf(820.65 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper addresses the problem of true delay estimation during high level design. The existing delay estimation techniques either estimate the topological delay of the circuit which may be pessimistic, or use gate-level timing analysis for calculating the true delay, which may be prohibitively expensive.We show that the paths in the implementation of a behavioral specification can be partitioned into two sets, SP and UP. While the paths in SP can affect the delay of the circuit ...

19 Error-tolerant design: SEU tolerant device, circuit and processor design

William Heidergott

June 2005 **Proceedings of the 42nd annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(364.56 KB) Additional Information: full citation, abstract, references, index terms

Development of highly reliable and available systems requires consideration of the occurrence of single event upsets, the effects they have on system performance, and strategies for their prevention and mitigation. Methods of systems engineering process and the application and validation of techniques for fault tolerance are discussed as elements in the elimination and mitigation of single event upsets.

Keywords: error detection and correction coding, fault avoidance, fault masking, fault tolerant systems, modular redundancy, radiation effects, single event upset, soft error rate, temporal redundancy

20 Incremental techniques for the identification of statically sensitizable critical paths

Yun-Cheng Ju, Resve A. Saleh

June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**

Publisher: ACM Press

Full text available: pdf(683.79 KB) Additional Information: full citation, references, citings, index terms

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	11	(path adj sensitization) and loop	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/28 10:30
L2	54	combinational near cycle	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/28 10:31
L3	77	combinational near cycle$1	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/28 10:37
L4	795	feedback near cycle	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/28 10:37
L5	548	L4 and @ad<"20010901"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/28 10:38
L6	154	L5 and sensiti$7	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/10/28 10:38